Claims 1, 3, 7-11 and 15-20 are rejected under 35 U.S.C. §112, second paragraph, as being indefinite.

The Office Action sets forth that the phrases "the printed circuit board on which said electronic device is mounted" in claim 1; "all four side edges of the die" in claims 8 and 16; and "all flanks of the die" in claim 18 lack sufficient literal antecedent basis.

Claim 1 has been amended to recite --a printed circuit board on which said electronic device is mounted--. Claim 1 has also been amended to include the phrase --silicon die having ... four side edges--, thereby providing antecedent basis for this limitation in claims 8 and 16.

With regard to claim 18, the phrase "all flanks of the die" has been changed to --the side edges of the die--.

Accordingly, the rejection is overcome and reconsideration and withdrawal of the rejection are requested.

* * *

Claims 1, 3, 7-10 and 17-20 are rejected under 35 U.S.C. §102(a) in the Office Action as being anticipated by Sato (U.S. Patent No. 5,519,251) or, in the alternative, under 35 U.S.C. §103(a) as being obvious based on a combination of Sato and Applicant's admitted prior art. Applicant traverses this rejection for the reasons set out below.

The Office Action asserts that Sato discloses every element of the claimed invention, or, when combined with Applicant's admitted prior art, renders the claimed invention obvious.

Applicant's invention, as described in claim 1, provides an electrically tested electronic device having connection pins wherein each of the connection pins includes a preformed portion which is not encapsulated in resin, in order to accommodate the thermal expansion difference between the silicon die and a printed circuit board on which said electronic device is mounted.

The Office Action specifically asserts that Sato discloses an arrangement wherein "each of said connection pins include a pre-formed portion 16.1 which is not encapsulated in said resin." However, Applicant respectfully submits that the Office Action mischaracterizes the teachings of Sato. As is generally well known in this art, "pre-formation" is a step carried out by leadframe manufacturers and entails formation of a shoulder bend formation which represent the pre-formed or pre-bent portion of the lead pin. The shoulder bend portion provides for the accommodation of a thermal expansion difference between the die and a printed circuit board by its flexing nature.

All of the embodiments described by Sato have the pre-formed or pre-bent portion encapsulated in the resin package. This is recognized by Sato in the discussion in column 10, lines 32-42, which sets forth

"However, if the external terminals 16 do not extend outwardly of the package 31 and is [sic] substantially embedded within the package 31, it is desirable to take some kind of measure to increase the strength of the semi-conductor device with respect to the stress which will be generated by the difference between the coefficients of thermal expansion of the leads 14 and the circuit substrate 48 on which the semiconductor device is mounted. Hence, this embodiment increases the surface area of the bottom surface 16a of the

external terminal 16 to increase the strength. In addition to increasing the strength, it is possible to facilitate the coating of an adhesive agent on the external terminal 16..."

Accordingly, the pre-formed or pre-bent portion of Sato, which is externally embedded in the device of Sato, is not involved in any way in thermal expansion difference accommodation. It is for this reason, Sato switches to an effort to increase the bonding strength through use of, for example, the dimples "16-1", cited in the Office Action. This dimpled expansion fails to represent a pre-formed or pre-bent portion for thermal expansion difference accommodation, as set forth in the claims.

Nor would it have been obvious to modify Sato to include a non-embedded arrangement relative to the embodiments relied upon in Sato in the Office Action. Sato specifically teaches away from using anything other than entirely encapsulated terminals except for the exposed bottom surface of the leads. (See, for example, lines 42-46 of the Summary of the Invention.) Also, one of the reasons set forth in Sato for fully encapsulating the terminal to leave only the exposed bottom surface concerns the perceived resin molding technique advantages described in column 3, lines 3-8 of Sato.

Reference is also made to the discussion on page 9, lines 11-15 of the present application concerning the earlier submitted "Int'l Journal of Microcircuits" article, showing the state of the art as being represented by completely bent around pins. This bent around formation and the completely embedded formation arrangement of Sato share some relationship with formation operating differences, such as between a chip manufacturer and a circuit board manufacturer. The dummy or pseudo-structure according to this invention

features the benefit of having both pre-formed and non-embedded pins which are mechanically and removably connected to the silicon die by connection means for removable attachment of said pins. This combination is not disclosed or suggested in the prior art.

The above Remarks overcome the outstanding rejection. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejection.

* * *

Claims 11, 15 and 16 are rejected under 35 U.S.C. §102(a) as being considered obvious based on a combination of Sato and Applicant's admitted prior art, and further in combination with McShane (U.S. Patent 5,311,057).

The deficiencies of Sato and Applicant's admitted prior art have been discussed above. Furthermore, McShane fails to remedy these deficiencies. Neither Sato nor McShane teach or fairly suggest a pre-formed portion which is not encapsulated in resin, to accommodate the thermal expansion difference between the silicon die and a printed circuit board on which said electronic device is mounted. The admitted prior art also fails to teach or fairly suggest this element of Applicant's invention. Moreover, there is nothing in the prior art of record that would motivate one of ordinary skill in the art to modify the teachings of Sato or McShane to incorporate this element of Applicant's invention.

The above Remarks overcome the outstanding rejection. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejection.

* * * * *

Also, upon allowance of generic claim 1, the reintroduction of those withdrawn claims depending from claim 1 is respectfully requested.

* * * * *

Applicant respectfully submits that this Amendment and the above Remarks overcome the outstanding rejections in this case and place the application in condition for immediate allowance. Allowance of this application is earnestly solicited. If, for any reason, there remains any outstanding obstacle to allowance (e.g., a remaining informality), the Examiner is invited to telephone the undersigned.

If any fees under 37 C.F.R. §§1.16 or 1.17 are due in this filing, please charge the fees to Deposit Account No. 02-4300; Order No. 033655.002.

If an extension of time under 37 C.F.R. §1.136 is necessary and not included herewith, such an extension is requested. The extension fee should be charged to Deposit Account No. 02–4300; Order No. 033655.002.

Respectfully submitted,

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Dated: November 27, 2001

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MARKED-UP PREVIOUS VERSION OF THE AMENDED CLAIMS

1. (Twice Amended) An electrically tested electronic device, free from infantile mortality, for direct mounting on a printed circuit board, wherein said electronic device comprises a silicon die having a top surface, [and] a bottom surface, and four side edges, in which an integrated circuit is realized externally accessible through a plurality of connection pads and an array of connection pins which are mechanically and removably connected to said silicon die by connected means for removable attachment of said pins, and are electrically connected to the connection pads of said silicon die by electric connection means, said electronic device being unpackaged or partially packaged in a resin, wherein each of said connection pins includes a pre-formed portion which is not encapsulated in said resin, in order to accommodate the thermal expansion difference between the silicon die and [the] a printed circuit board on which said electronic device is mounted.

18. (Amended) An electronic device according to claim 1, wherein said electronic device is partially packaged in a resin so as to comprise a semi-package, that covers a first surface of the die where said connection pads are arranged together with said connection means between said connection pins and the connection pads, as well as all [flanks] side edges of the die, leaving an opposite, second surface of the die exposed.

CLEAN COPY OF THE AMENDED CLAIMS

1. (Twice Amended) An electrically tested electronic device, free from infantile mortality, for direct mounting on a printed circuit board, wherein said electronic device comprises a silicon die having a top surface, a bottom surface, and four side edges, in which an integrated circuit is realized externally accessible through a plurality of connection pads and an array of connection pins which are mechanically and removably connected to said silicon die by connection means for removable attachment of said pins, and are electrically connected to the connection pads of said silicon die by electric connection means, said electronic device being unpackaged or partially packaged in a resin, wherein each of said connection pins includes a pre-formed portion which is not encapsulated in said resin, in order to accommodate the thermal expansion difference between the silicon die and a printed circuit board on which said electronic device is mounted.

18. (Amended) An electronic device according to claim 1, wherein said electronic device is partially packaged in a resin so as to comprise a semi-package, that covers a first surface of the die where said connection pads are arranged together with said connection means between said connection pins and the connection pads, as well as all side edges of the die, leaving an opposite, second surface of the die exposed.

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